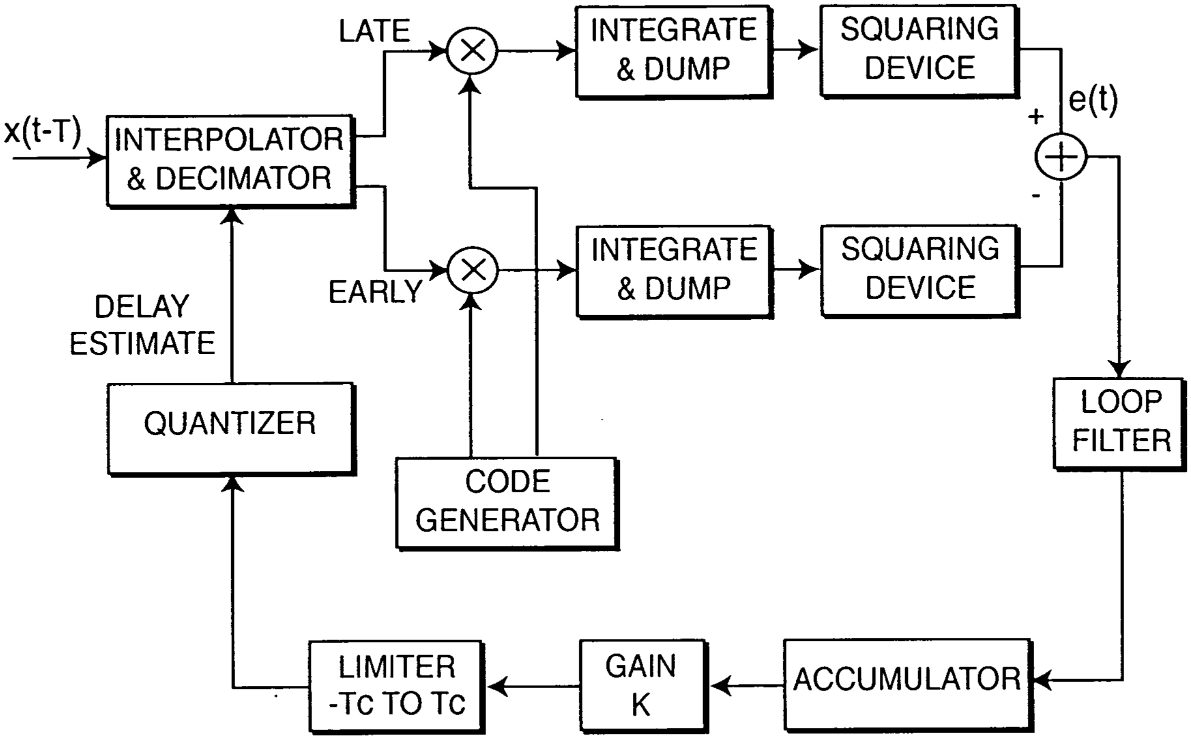

FIG. 1
PRIOR ART

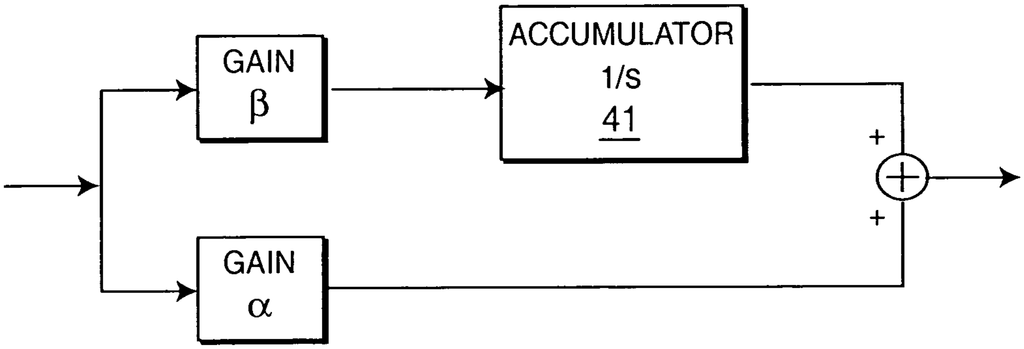

FIG. 4

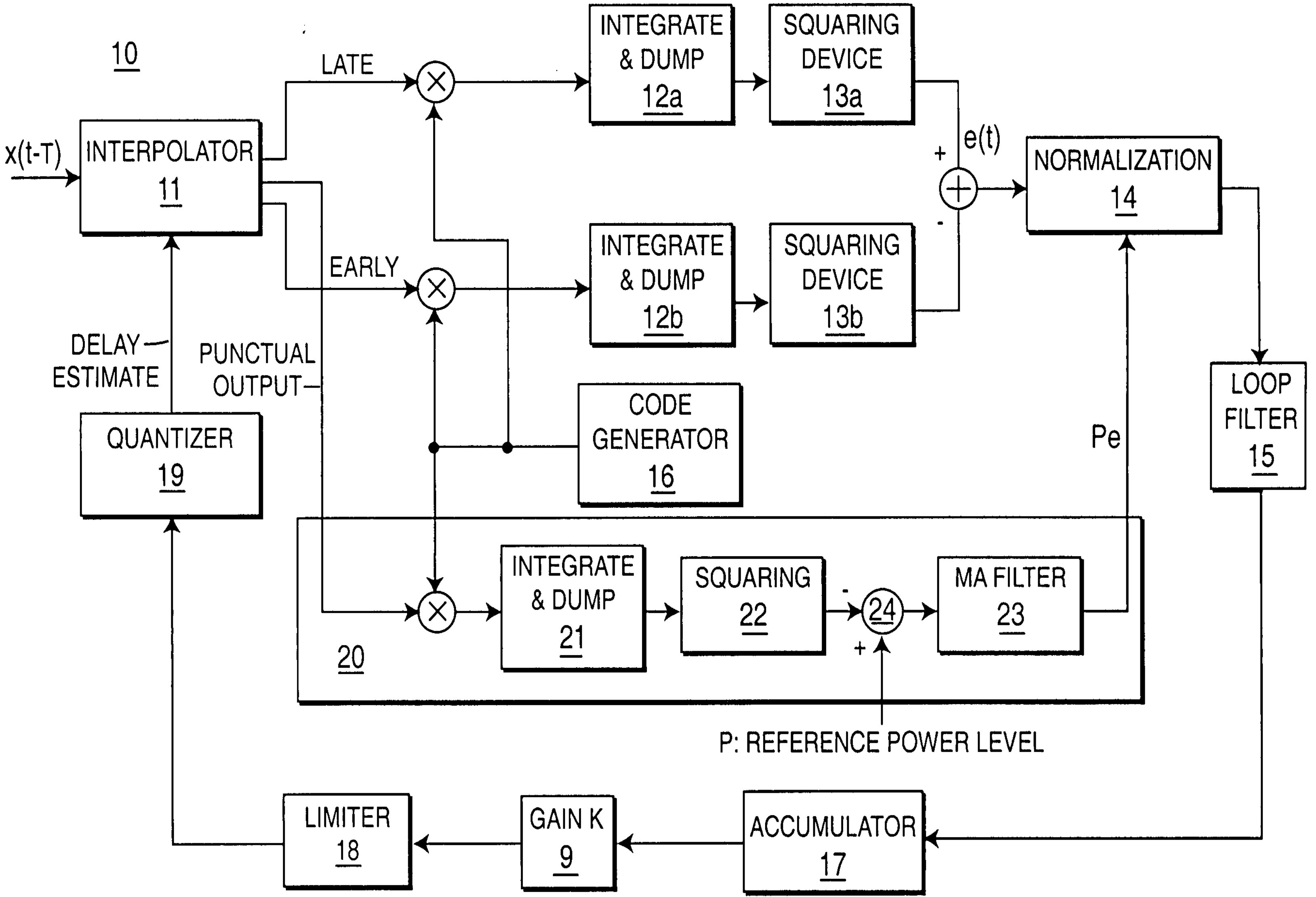
10
x(t-T)
INTERPOLATOR
11
LATE
EARLY
DELAY
ESTIMATE
PUNCTUAL
OUTPUT
QUANTIZER
19
INTEGRATE
& DUMP
12a
SQUARING
DEVICE
13a
INTEGRATE
& DUMP
12b
SQUARING
DEVICE
13b
+
-
e(t)
NORMALIZATION
14
CODE
GENERATOR
16
Pe
LOOP
FILTER
15
INTEGRATE
& DUMP
21
SQUARING
22
-
+
24
MA FILTER
23
20
P: REFERENCE POWER LEVEL
LIMITER
18
GAIN K
9
ACCUMULATOR
17

FIG. 2

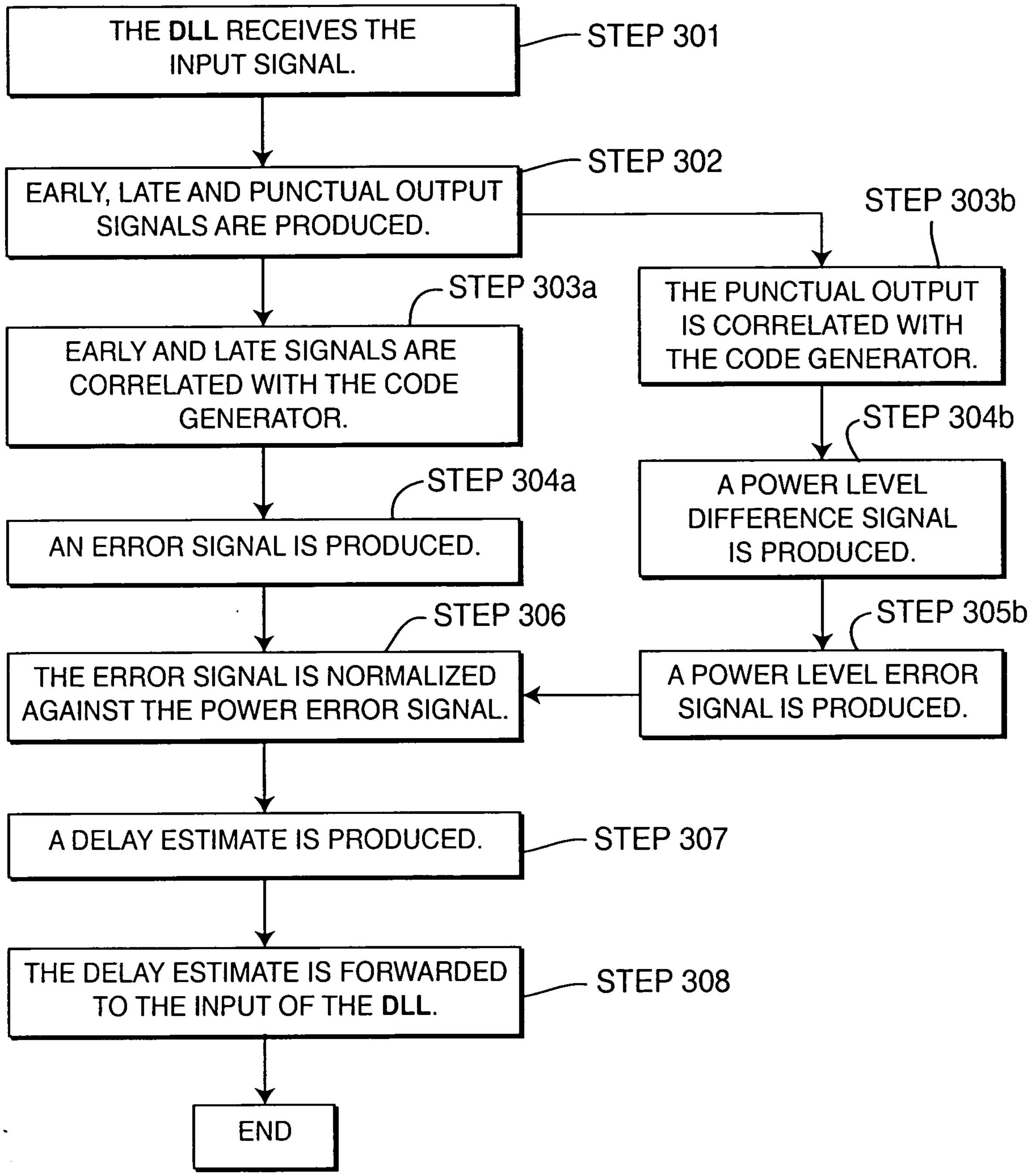
THE DLL RECEIVES THE INPUT SIGNAL.
STEP 301
EARLY, LATE AND PUNCTUAL OUTPUT SIGNALS ARE PRODUCED.
STEP 302
STEP 303b
THE PUNCTUAL OUTPUT IS CORRELATED WITH THE CODE GENERATOR.
STEP 303a
EARLY AND LATE SIGNALS ARE CORRELATED WITH THE CODE GENERATOR.
STEP 304b
A POWER LEVEL DIFFERENCE SIGNAL IS PRODUCED.
STEP 304a
AN ERROR SIGNAL IS PRODUCED.
STEP 306
STEP 305b
THE ERROR SIGNAL IS NORMALIZED AGAINST THE POWER ERROR SIGNAL.
A POWER LEVEL ERROR SIGNAL IS PRODUCED.
A DELAY ESTIMATE IS PRODUCED.
STEP 307
THE DELAY ESTIMATE IS FORWARDED TO THE INPUT OF THE DLL.
STEP 308
END

FIG. 3